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EXAMINER	
NG, CHRISTINE Y	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,728	DENTON ET AL.	
	Examiner	Art Unit	
	Christine Ng	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,25-32 and 38-45* is/are rejected.

7)☒ Claim(s) *21-24 and 33-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 16 objected to because of the following informalities:

In line 11, "g)" should be changed to "h)".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 38-45 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how the components of claim 38 are connected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,515,967 to Wei et al.

Referring to claim 25, Wei discloses a method of testing network communications equipment, comprising:

a) Programming a first set of registers (MRM testers) that define a format of a first test packet (Figure 10). Refer to Column 5, lines 57-64 and Column 11, lines 29-56.

b) Programming a second set of registers (MRM testers) that define a format of second test packet (Figure 10). Refer to Column 5, lines 57-64 and Column 11, lines 29-56.

c) Transmitting a synchronization packet (Figure 7, beacon message). The beacon message is sent by the MRM manager, which is identified by the "synchronization source identifier" (Column 9, lines 7-10).

d) Transmitting the first test packet (Figure 10). Refer to Column 10, lines 25-27.

e) Transmitting, after a first inter-packet gap (Figure 8, interpacket delay 825), the second test packet (Figure 10). Refer to Column 10, lines 25-27.

Wherein the first test packet (Figure 10) comprises a first packet header (Figure 6), and a first payload (Figure 10); and the second test packet (Figure 10) comprises a second packet header (Figure 6), and a second payload (Figure 10). Refer to Column 7, line 31 to Column 8, line 46 and Column 11, lines 29-56.

Referring to claim 26, Wei et al discloses that the first and second packet headers (Figure 6) are different. The fields 601-623 of the header in Figure 6 can contain different contents. Refer to Column 7, line 31 to Column 8, line 46.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,228,042 to Gauthier et al in view of U.S. Patent No. 6,034,948 to Nakamura et al.

Referring to claim 1, Gauthier et al disclose in Figure 1 a network communications system, comprising:

A switch (circuit under test 20) having a first plurality of ports (X, Y). The circuit under test 20 comprises a plurality of X input ports and Y output ports. Refer to Column 2, lines 6-11.

A line card (Figure 1) coupled to at least one of the ports (X, Y).

Wherein each line card (Figure 1) includes a test generator, each test generator comprising a test pattern generator (LFSR 5) operable to produce and transmit at least two traffic flows (10-bit output test patterns), and further comprising a receiver (LFSR 50) operable to produce at least two expected traffic flows (10-bit test patterns), to receive at least two transmitted traffic flows (10-bit output test patterns) and to compare (comparator 60) the received traffic flows (10-bit output test patterns) to the expected traffic flows (10-bit test patterns). Refer to Column 3, lines 22-32 and lines 55-60 and Column 3, line 66 to Column 4, line 2.

Gauthier et al do not disclose a plurality of line cards.

Nakamura et al disclose in Figure 1 a plurality of line cards (testers A-D) coupled to a corresponding port of the switch (repeating installation 1). A system having a plurality of line cards coupled to at least one of the ports allows simultaneous testing of several ports of the switch. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of line cards, the motivation being that this saves times by allowing several ports of the switch to be tested for synchronization at the same time.

Referring to claim 2, Gauthier et al disclose in Figure 2 that each test pattern generator (LFSR 5,50) further comprises a plurality of registers (shift register 10,51) which define the size (10-bits) and contents (bits) of the at least two traffic flows (10-bit test patterns). Refer to Column 3, lines 12-17 and Column 4, lines 14-41.

Referring to claim 3, Gauthier et al disclose in Figure 2 that each test pattern generator (LFSR 5,50) comprises a state machine (shift register 10,51 and EX_OR 13,53) for controlling the construction and transmission of the at least two traffic flows (10-bit test patterns). Refer to Column 3, lines 12-17 and Column 4, lines 14-41.

However, Gauthier et al do not disclose that the state machine also controls the insertion of unique packet headers into each of the at least two traffic flows.

Nakamura et al disclose in Figure 8A that each of the at least two traffic flows (Figure 6B, test data TD0, TD1, TD2...) includes a packet header and each of the packet headers are different. The fields of the header in Figure 8A can contain different contents. Refer to Column 9, lines 32-41. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to include that the state machine also controls the insertion of unique packet headers into each of the at least two traffic flows, the motivation being that test packets must have unique headers in order to distinguish between them during a test.

Referring to claim 4, Gauthier et al disclose in Figure 1 that the received traffic flows (10-bit output test patterns) originate at one of the first plurality of ports (X on circuit under test 20), and are received from a second one of the first plurality of ports (Y on circuit under test 20). Refer to Column 3, lines 22-32 and lines 55-65.

Referring to claim 5, Gauthier et al disclose in Figure 1 that the test generator is integrated on a single chip, the single chip being disposed on the line card (Figure 1). "Since the circuit uses only digital logic circuitry, it may be readily implemented as an integrated circuit either on its own or as a portion of another integrated circuit" (Column 5, lines 12-15).

8. Claims 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,034,948 to Nakamura et al in view of U.S. Patent No. 5,228,042 to Gauthier et al.

Referring to claim 6, Nakamura et al disclose in Figures 1 and 2 a method of full speed in-circuit testing of a multi-port network communication switch, comprising:

Coupling, to each port (P0-P7) of the multi-port communication switch (repeating installation 1), one of a first plurality of line cards (transmitter-receivers 3,4), each line card (transmitter-receivers 3,4) comprising a test generator (tester 10,11), and each test

generator comprising a test packet transmitter (test packet transmitter 22) or a test packet receiver (test packet receiving/verifying unit 23). Refer to Column 5, lines 49-62.

Operating a first test generator (tester 10) coupled to a first port (P2) of the multi-port communication switch (repeating installation 1), to generate at least two traffic flows (Figure 6B, test data TD0, TD1, TD2...) destined for a second port (P5) of the multi-port communication switch (repeating installation 1), and to transmit those at least two traffic flows. Refer to Column 6, line 54 to Column 7, line 23.

Operating a second test generator (tester 11) coupled to the second port (P5) to generate a local copy of at least two expected traffic flows, to receive the at least two traffic flows (Figure 6B, test data TD0, TD1, TD2...), and to compare the at least two expected traffic flows with the at least two received traffic flows (Figure 6B, test data TD0, TD1, TD2...). Refer to Column 8, lines 13-21.

Nakamura et al do not disclose that each test generator (tester 10,11) comprises both a test packet transmitter (test packet transmitter 22) and a test packet receiver (test packet receiving/verifying unit 23).

Gauthier et al disclose in Figure 1 a test generator that includes both a test packet transmitter (LFSR 5) and a test packet receiver (LFSR 50) connected to a switch (circuit under test 20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each test generator comprises both a test packet transmitter and a test packet receiver, the motivation being so that the test generator can serve as a transmission tester and a reception tester to allow testing in both directions.

Referring to claim 7, Nakamura et al disclose in Figure 2 recording an error if any one of the at least two received traffic flows (Figure 6B, test data TD0, TD1, TD2...) do not match the expected flows. Error is detected by determining whether or not an expected value code C is correct. If there is an error, it is displayed on console 13. Refer to Column 9, line 42 to Column 10, line 1 and Column 11, lines 58-61.

Referring to claim 8, Nakamura et al do not disclose transmitting a synchronization packet from the first test generator coupled to the first port to the second test generator coupled to the second port.

Gauthier et al disclose in Figure 1 transmitting a synchronization packet (using test patterns and a seed value) from the first test generator (LFSR 5) coupled to the first port (X) to the second test generator (LFSR 50) coupled to the second port (Y). Refer to Column 2, lines 6-31. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include transmitting a synchronization packet from the first test generator coupled to the first port to the second test generator coupled to the second port, the motivation being in order to synchronize the two ports to allow data transmission between them.

Referring to claim 9, Nakamura et al disclose in Figure 1 that the first port (P2) and the second port (P5) are different ports of the switch (repeating installation 1).

Referring to claim 10, Nakamura et al disclose in Figure 8A that each of the at least two traffic flows (Figure 6B, test data TD0, TD1, TD2...) includes a packet header and each of the packet headers are different. The fields of the header in Figure 8A can contain different contents. Refer to Column 9, lines 32-41.

Referring to claim 11, Nakamura et al do not disclose setting a flag indicative of an out-of-synchronization state; receiving at least one packet; comparing the at least one packet to an expected pattern, and setting a flag indicative of a synchronized state if the comparison of the received and expected data results in a match.

Gauthier et al disclose in Figure 1 that the test generator is initially out of synchronization. The second test generator (LFSR 50) receives at least one packet (test pattern) from the first test generator (LFSR 5); compares the at least one packet (test pattern) to an expected pattern (generated at LFSR 50), and sets a flag indicative of a synchronization state if the comparison of the received and expected data results in a match (using a seed value). Refer to Column 2, lines 6-27 and Abstract. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include setting a flag indicative of an out-of-synchronization state; receiving at least one packet; comparing the at least one packet to an expected pattern, and setting a flag indicative of a synchronized state if the comparison of the received and expected data results in a match, the motivation being in order to synchronize the system for proper transmission and reception of data.

Referring to claim 12, Nakamura et al disclose in Figure 8A that an end of packet flag (E) is received at the end of a packet. Refer to Column 9, lines 40-41.

Referring to claim 13, Nakamura et al disclose in Figure 8A that the at least one packet comprises a first predetermined integer number (L) of packets (bytes). Refer to Column 9, lines 36-37.

Referring to claim 14, Nakamura et al do not disclose setting the flag indicative of an out-of-synchronization state if a second predetermined integer number of packets fail to match the expected data.

Gauthier et al disclose in Figure 1 that a comparator 60 compares the test patterns generated by test generator LFSR 5 and sets a flag (error condition) indicative of an out-of-synchronization state if a second predetermined integer number (1) of packets fail to match the expected data (test patterns generated by test generator LFSR 50). Refer to Abstract and Column 5, lines 6-9. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include setting the flag indicative of a out-of-synchronization state if a second predetermined integer number of packets fail to match the expected data, the motivation being to provide notification of when the system is not synchronized in order to facilitate data transmission.

Referring to claim 15, Nakamura et al disclose programming at least one packet header (Figure 8A) for the test packet transmitter (Figure 2, test packet transmitter 22), and programming at least one packet header (Figure 8A) for the test packet receiver (Figure 2, test packet receiving/verifying unit 23). Refer to Column 8, lines 13-21 and Column 9, lines 32-41.

9. Claims 16-20 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,515,967 to Wei et al in view of U.S. Patent No. 6,522,661 to Min.

Referring to claim 16, refer to the rejection of claims 25-26 for the rejection of steps (a)-(g) and wherein the first header is different from the second header.

Wei et al do not disclose step (h): repeating steps (b) though (g) at least once. Min discloses in Figure 1 node S1 and node Sm exchanging packets and in Figure 2 node A and node B contending for access to a channel. Refer to Column 1, lines 27-34 and Column 2, lines 10-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include step (h): repeating steps (b) though (g) at least once, the motivation being in order to allow two nodes to take turns alternatively transmitting packets to each other.

Referring to claim 17, Wei et al do not disclose that the first length and the second length are different.

Min et al discloses in Figure 2 that the interpacket gaps between node A and node B are of different lengths: IPG + 0xslot time and IPG + 1xslot time. Refer to Column 2, lines 10-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the first length and the second length are different, the motivation being so that the packets will not collide with each other during transmission on the same channel.

Referring to claim 18, Wei et al disclose in Figure 10 that the first payload and the second payload are different. The fields 1003-1017 of the test packet can contain different contents. Refer to Column 11, lines 29-56.

Referring to claim 19, Wei et al disclose in Figure 8 counting the number of packets transmitted by the test generator (MRM testers). "A field 803 contains a total

packet count 805 indicating a total number of packets to be sent by the test sender" (Column 10, lines 5-8).

Referring to claim 20, Wei et al disclose in Figure 11 that transmitting from the test packet generator (primary storage 1104) comprises communicating data onto a parallel bus (memory bus 1108). Refer to Column 12, lines 21-50.

Referring to claims 27 and 28, refer to the rejection of claims 16 and 17.

Referring to claims 29 and 30, refer to the rejection of claim 18.

Referring to claims 31 and 32, Wei et al disclose programming the first/second set of registers (MRM testers) comprises writing data into one or more registers so as to define:

1) a total number of bytes (Figure 6, data length 619) in the first/second test packet. Refer to Column 8, lines 1-3.

2) a size of a gap (Figure 8, interpacket delay 825) between the transmission of the first and second test packets. Refer to Column 10, lines 25-27.

3) a pattern (Figure 10) used to fill the first/second payload. Refer to Column 11, lines 29-56.

4) a content of the first/second header (Figure 6). Refer to Column 7, line 31 to Column 8, line 46.

Allowable Subject Matter

10. Claims 21-24 and 33-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng
January 27, 2004

RICKY NGO
PRIMARY EXAMINER